

# HM628128 Series

---

## 131072-word × 8-bit High Speed CMOS Static RAM

The Hitachi HM628128 is a CMOS static RAM organized 128-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology.

It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. The TSOP package is suitable for cards, and reverse type TSOP is also provided.

### Features

- High speed: fast access time 70/85/100/120 ns (max)
- Low power
  - Standby: 10 μW (typ) (L/L-L/L-SL version)
  - Operation: 75 mW (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L/L-L/L-SL version) (2 chip selection for battery back up)

5

4496203 0024973 218

HITACHI

Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

5-39

# HM628128 Series

## Ordering Information

Type No.	Access time	Package	Type No.	Access time	Package
HM628128P-7	70 ns	600-mil,	HM628128FP-7	70 ns	525 mil,
HM628128P-8	85 ns	32-pin plastic	HM628128FP-8	85 ns	32-pin plastic
HM628128P-10	100 ns	DIP (DP-32)	HM628128FP-10	100 ns	SOP (FP-32D)
HM628128P-12	120 ns		HM628128FP-12	120 ns	
HM628128LP-7	70 ns		HM628128LFP-7	70 ns	
HM628128LP-8	85 ns		HM628128LFP-8	85 ns	
HM628128LP-10	100 ns		HM628128LFP-10	100 ns	
HM628128LP-12	120 ns		HM628128LFP-12	120 ns	
HM628128LP-7SL	70 ns		HM628128LFP-7SL	70 ns	
HM628128LP-8SL	85 ns		HM628128LFP-8SL	85 ns	
HM628128LP-10SL	100 ns		HM628128LFP-10SL	100 ns	
HM628128LP-12SL	120 ns		HM628128LFP-12SL	120 ns	
HM628128T-7	70 ns	8mm x 20mm	HM628128R-7	70 ns	8mm x 20 mm
HM628128T-8	85 ns	32-pin TSOP	HM628128R-8	85 ns	32-pin TSOP
HM628128T- 10	100 ns	(normal type)	HM628128R-10	100 ns	(reverse type)
HM628128T- 12	120 ns	(TFP-32D)	HM628128R- 12	120 ns	(TFP-32DR)
HM628128LT-7	70 ns		HM628128LR-7	70 ns	
HM628128LT-8	85 ns		HM628128LR-8	85 ns	
HM628128LT-10	100 ns		HM628128LR-10	100 ns	
HM628128LT-12	120 ns		HM628128LR-12	120 ns	
HM628128LT-7L	70 ns		HM628128LR-7L	70 ns	
HM628128LT-8L	85 ns		HM628128LR-8L	85 ns	
HM628128LT-10L	100 ns		HM628128LR-10L	100 ns	
HM628128LT-12L	120 ns		HM628128LR-12L	120 ns	
HM628128LT-7SL	70 ns		HM628128LR-7SL	70 ns	
HM628128LT-8SL	85 ns		HM628128LR-8SL	85 ns	
HM628128LT-10SL	100 ns		HM628128LR-10SL	100 ns	
HM628128LT-12SL	120 ns		HM628128LR-12SL	120 ns	

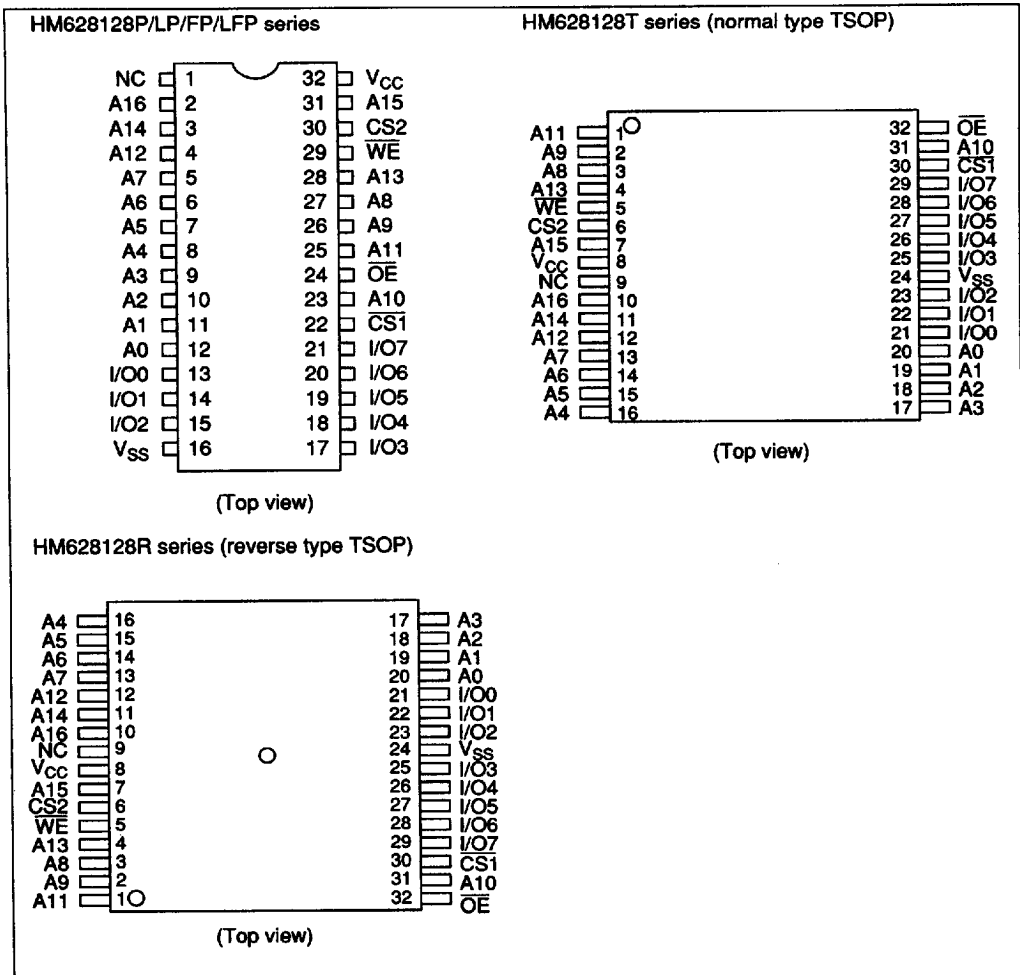
4496203 0024974 154

HITACHI

5-40

Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

## Pin Arrangement



## Pin Description

Pin name	Function	Pin name	Function
A0–A16	Address	OE	Output enable
I/O0–I/O7	Input/output	NC	Not connected
CS1	Chip select 1	V <sub>CC</sub>	Power supply
CS2	Chip select 2	V <sub>SS</sub>	Ground
WE	Write enable		

4496203 0024975 090

**HITACHI**

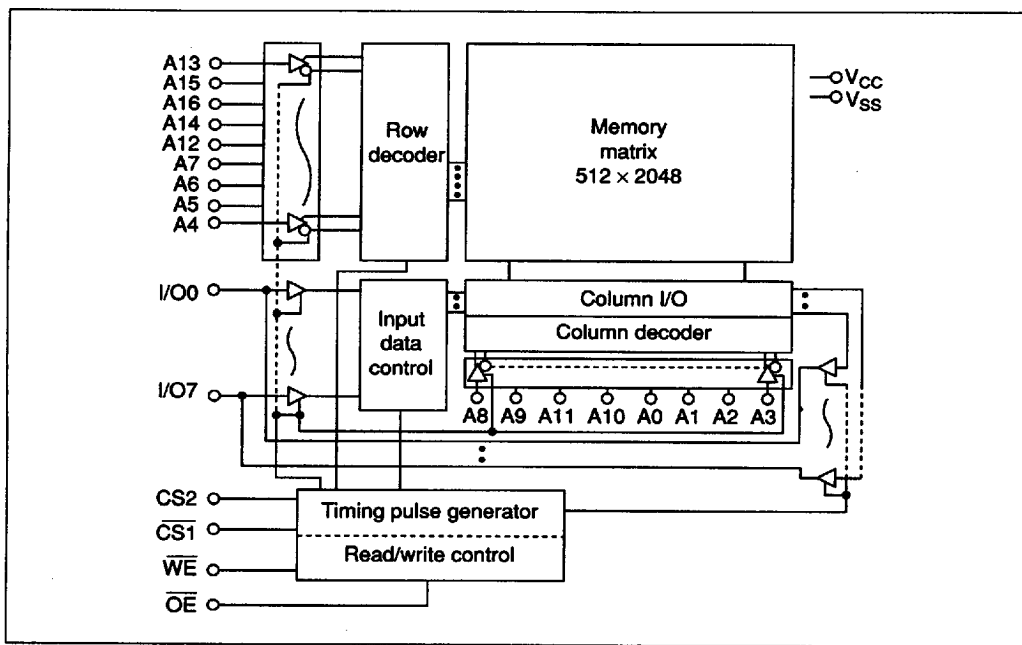
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

5-41



# HM628128 Series

## Block Diagram



### Truth Table

$\overline{WE}$	$\overline{CS1}$	$CS2$	$\overline{OE}$	Mode	$V_{CC}$ current	Dout pin	Cycle
x	H	x	x	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
x	x	L	x		$I_{SB}, I_{SB1}$	High-Z	—
H	L	H	H	Output disable	$I_{CC}$	High-Z	—
H	L	H	L	Read	$I_{CC}$	Dout	Read cycle
L	L	H	H	Write	$I_{CC}$	$D_{IN}$	Write cycle (1)
L	L	H	L		$I_{CC}$	$D_{IN}$	Write cycle (2)

Note: x: H or L

4496203 0024976 T27

HITACHI

5-42

Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V <sub>SS</sub>	V <sub>T</sub>	-0.5* to +7.0	V
Power dissipation	P <sub>T</sub>	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +125	°C
Storage temperature under bias	Tbias	-10 to +85	°C

Note: -3.0 V for pulse half-width ≤ 30 ns

**Recommended DC Operating Conditions (Ta = 0 to +70°C)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
	V <sub>SS</sub>	0	0	0	V
Input high (logic 1) voltage	V <sub>IH</sub>	2.2	—	6.0	V
Input low (logic 0) voltage	V <sub>IL</sub>	-0.3*	—	0.8	V

Note: -3.0 V for pulse half-width ≤ 30 ns

4496203 0024977 963

**HITACHI**

Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

## HM628128 Series

DC Characteristics ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Min	Typ <sup>1</sup>	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	2	$\mu\text{A}$	$V_{IN} = V_{SS}$ to $V_{CC}$
Output leakage current	$ I_{LO} $	—	—	2	$\mu\text{A}$	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $OE = V_{IH}$ or $WE = V_{IL}$ , $V_{IO} = V_{SS}$ to $V_{CC}$
Operating power supply current: DC	$I_{CC}$	—	15	35	mA	$\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ , others = $V_{IH}/V_{IL}$ , $I_{VO} = 0$ mA
Operating power supply current	$I_{CC1}$	—	45	70	mA	Min. cycle, duty = 100%, $\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ , others = $V_{IH}/V_{IL}$ $I_{VO} = 0$ mA
	$I_{CC2}$	—	15	30	mA	Cycle time = 1 $\mu\text{s}$ , duty = 100%, $I_{VO} = 0$ mA, $\overline{CS1} \leq 0.2\text{ V}$ , $CS2 \geq V_{CC} - 0.2\text{ V}$ , $V_{IH} \geq V_{CC} - 0.2\text{ V}$ , $V_{IL} \leq 0.2\text{ V}$
Standby power supply current: DC	$I_{SB}$	—	1	3	mA	$\overline{CS1} = V_{IH}$ , $CS2 = V_{IH}$ or $CS2 = V_{IL}$
Standby power supply current (1): DC	$I_{SB1}$	—	0.02	2	mA	$V_{IN} \geq 0\text{ V}$ , $\overline{CS1} \geq V_{CC} - 0.2\text{ V}$ , $CS2 \geq V_{CC} - 0.2\text{ V}$ or $0\text{ V} \leq CS2 \leq V_{IL}$
		—	$2^{\cdot 2}$	$100^{\cdot 2}$	$\mu\text{A}$	
		—	$2^{\cdot 3}$	$50^{\cdot 3}$	$\mu\text{A}$	
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2.1\text{ mA}$
Output high voltage	$V_{OH}$	2.4	—	—	V	$I_{OH} = -1.0\text{ mA}$

- Note: 1. Typical values are at  $V_{CC} = 5.0\text{ V}$ ,  $T_a = +25^\circ\text{C}$  and specified loading.  
2. These characteristics are guaranteed only for L-version.  
3. These characteristics are guaranteed only for L-L/L-SL version.

Capacitance ( $T_a = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	$C_{in}$	—	—	8	pF	$V_{IN} = 0\text{ V}$
Input/output capacitance	$C_{IO}$	—	—	10	pF	$V_{IO} = 0\text{ V}$

Note: These parameters are sampled and not 100% tested.

4496203 0024978 8TT

HITACHI

5-44

Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

## AC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, unless otherwise noted)

### Test Conditions:

- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing reference: 1.5 V
- Input rise and fall times: 5 ns
- Output load: 1 TTL gate and C<sub>L</sub> (100 pF) (Including scope and jig)

### Read Cycle

Parameter	Symbol	HM628128-7		HM628128-8		HM628128-10		HM628128-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read cycle time	t <sub>RC</sub>	70	—	85	—	100	—	120	—	ns
Address access time	t <sub>AA</sub>	—	70	—	85	—	100	—	120	ns
Chip selection (CS1) to output valid	t <sub>CO1</sub>	—	70	—	85	—	100	—	120	ns
Chip selection (CS2) to output valid	t <sub>CO2</sub>	—	70	—	85	—	100	—	120	ns
Output enable (OE) output valid	t <sub>OE</sub>	—	35	—	45	—	50	—	60	ns
Chip selection (CS1) to output in low-Z <sup>1,2,3</sup>	t <sub>LZ1</sub>	10	—	10	—	10	—	10	—	ns
Chip selection (CS2) to output in low-Z <sup>1,2,3</sup>	t <sub>LZ2</sub>	10	—	10	—	10	—	10	—	ns
Output enable (OE) to output in low-Z <sup>1,2,3</sup>	t <sub>OLZ</sub>	5	—	5	—	5	—	5	—	ns
Chip deselection (CS1) to output in high-Z <sup>1,2,3</sup>	t <sub>HZ1</sub>	0	25	0	30	0	35	0	45	ns
Chip deselection (CS2) to output in high-Z <sup>1,2,3</sup>	t <sub>HZ2</sub>	0	25	0	30	0	35	0	45	ns
Output disable (OE) to output in high-Z <sup>1,2,3</sup>	t <sub>OHZ</sub>	0	25	0	30	0	35	0	45	ns
Output hold from address change	t <sub>OH</sub>	10	—	10	—	10	—	10	—	ns

- Notes: 1. t<sub>HZ</sub> and t<sub>OHZ</sub> are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.  
 2. At any given temperature and voltage condition, t<sub>HZ</sub> max is less than t<sub>LZ</sub> min both for a given device and from device to device.  
 3. These parameters are sampled and not 100% tested.

4496203 0024979 736

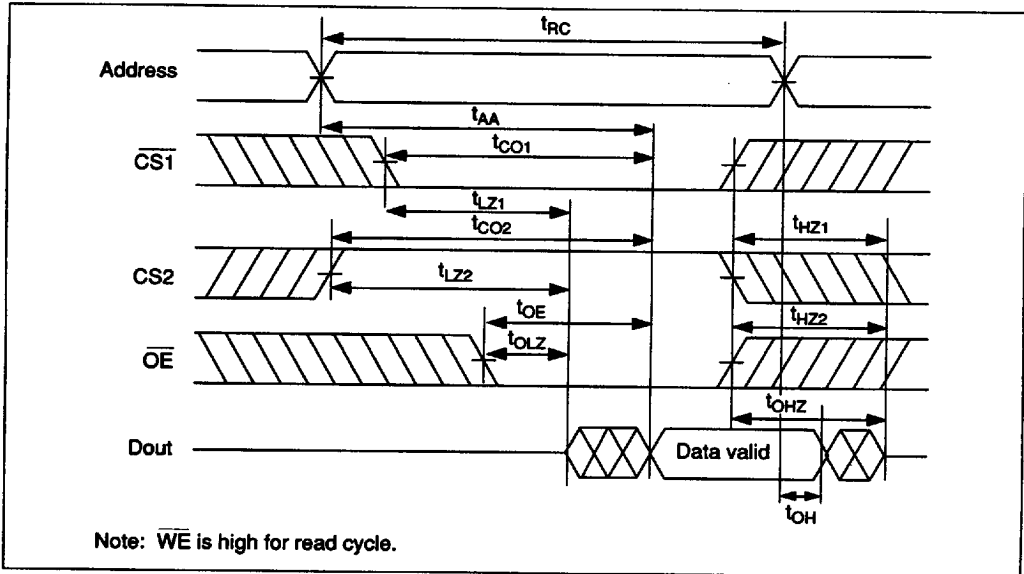
**HITACHI**

Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

5-45

# HM628128 Series

## Read Timing Waveform



## Write Cycle

Parameter	Symbol	HM628128-7		HM628128-8		HM628128-10		HM628128-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write cycle time	$t_{WC}$	70	—	85	—	100	—	120	—	ns
Chip selection to end of write	$t_{CW}$	60	—	75	—	80	—	85	—	ns
Address setup time	$t_{AS}$	0	—	0	—	0	—	0	—	ns
Address valid to end of write	$t_{AW}$	60	—	75	—	80	—	85	—	ns
Write pulse width	$t_{WP}$	50	—	55	—	60	—	70	—	ns
Write recovery time <sup>*1</sup>	$t_{WR}$	5	—	5	—	5	—	10	—	ns
		10	—	10	—	10	—	15	—	ns <sup>*1</sup>
Write to output in high-Z <sup>2</sup>	$t_{WHZ}$	0	25	0	30	0	35	0	40	ns
Data to write time overlap	$t_{DW}$	30	—	35	—	40	—	45	—	ns
Write hold from write time	$t_{DH}$	0	—	0	—	0	—	0	—	ns
Output active from end of write <sup>*1</sup>	$t_{OW}$	5	—	5	—	5	—	5	—	ns

Notes: 1. This value is measured from CS2 going low to the end of write cycle.  
2. This parameter is sampled and not 100% tested.

4496203 0024980 458

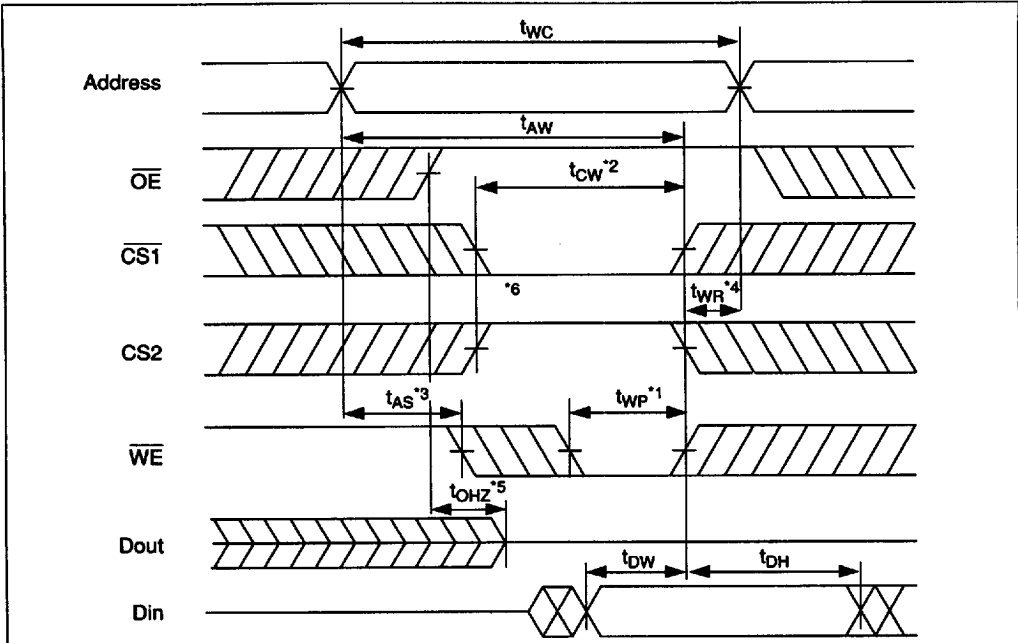
HITACHI

5-46

Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300



Write Timing Waveform (1) ( $\overline{OE}$  Clock)

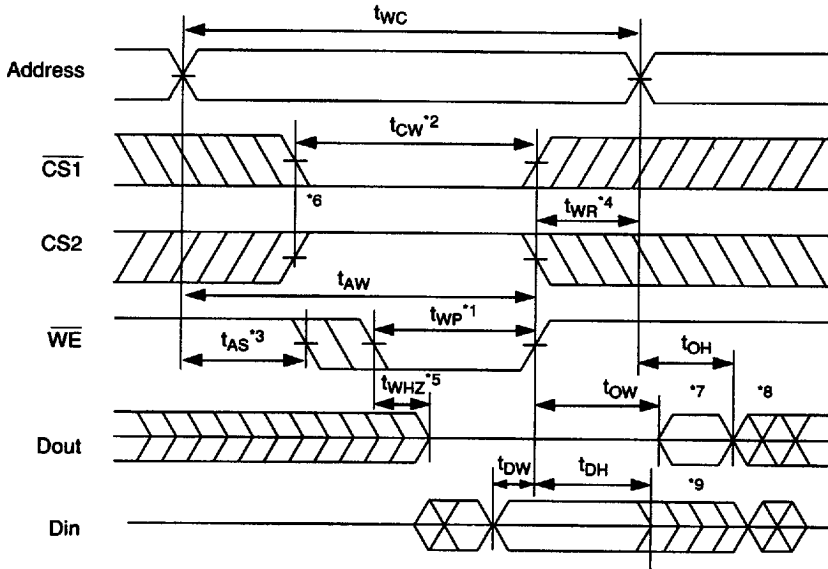


- Notes:
1. A write occurs during the overlap of a low  $\overline{CS1}$ , a high  $\overline{CS2}$ , and a low  $\overline{WE}$ . A write begin at the latest transition among  $\overline{CS1}$  going low,  $\overline{CS2}$  going high and  $\overline{WE}$  going low. A write end at the earliest transition among  $\overline{CS1}$  going high,  $\overline{CS2}$  going low and  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  2.  $t_{CW}$  is measure from the later of  $\overline{CS1}$  going low or  $\overline{CS2}$  going high to the end of write.
  3.  $t_{AS}$  is measured from the address valid to the beginning of write.
  4.  $t_{WR}$  is measured from the earliest of  $\overline{CS1}$  or  $\overline{WE}$  going high or  $\overline{CS2}$  going low to the end of write cycle.
  5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
  6. If  $\overline{CS1}$  goes low simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the outputs remain in high impedance state.

5

# HM628128 Series

## Write Timing Waveform (2) ( $\overline{OE}$ Fixed Low)



- Notes:
1. A write occurs during the overlap of a low  $\overline{CS1}$ , a high  $CS2$ , and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS1}$  going low,  $CS2$  going high and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS1}$  going high,  $CS2$  going low and  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.  $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$
  2.  $t_{CW}$  is measured from the later of  $\overline{CS1}$  going low or  $CS2$  going high to the end of write.
  3.  $t_{AS}$  is measured from the address valid to the beginning of write.
  4.  $t_{WR}$  is measured from the earliest of  $\overline{CS1}$  or  $\overline{WE}$  going high or  $CS2$  going low to the end of write cycle.
  5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
  6. If  $\overline{CS1}$  goes low simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the outputs remain in high impedance state.
  7.  $Dout$  is the same phase of the latest written data in this write cycle.
  8.  $Dout$  is the read data of next address.
  9. If  $\overline{CS1}$  is low and  $CS2$  is high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.

4496203 0024982 220

HITACHI

5-48

Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

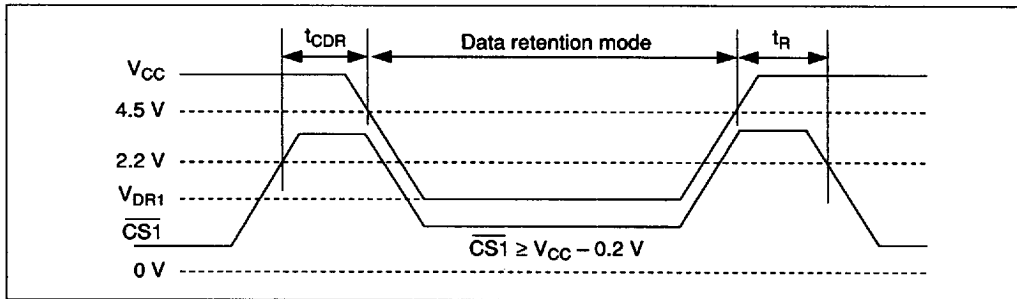
Low  $V_{CC}$  Data Retention Characteristics ( $T_a = 0$  to  $+70^{\circ}\text{C}$ )

(These characteristics are guaranteed only for L, L-L, and L-SL version.)

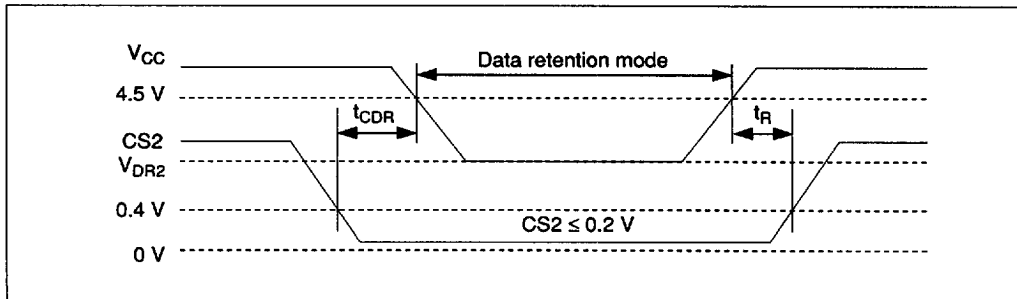
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*4	
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$\overline{CS1} \geq V_{CC} - 0.2\text{V}$ , $CS2 \geq V_{CC} - 0.2\text{V}$ , or $0\text{V} \leq CS2 \leq 0.2\text{V}$ , $V_{in} \geq$	
Data retention current	$I_{CCDR}$	L	—	1	$50^1$	$\mu\text{A}$	$V_{CC} = 3.0\text{V}$ , $V_{in} \geq 0\text{V}$ , $\overline{CS1} \geq V_{CC} - 0.2\text{V}$ , $CS2 \geq V_{CC} - 0.2\text{V}$ , or $0\text{V} \leq CS2 \leq 0.2\text{V}$
		L-L	—	1	$30^2$	$\mu\text{A}$	
		L-SL	—	1	$15^3$	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform	
Operation recovery time	$t_R$	5	—	—	ms		

- Notes: 1. 20  $\mu\text{A}$  max at  $T_a = 0$  to  $40^{\circ}\text{C}$   
 2. 6  $\mu\text{A}$  max at  $T_a = 0$  to  $40^{\circ}\text{C}$   
 3. 3  $\mu\text{A}$  max at  $T_a = 0$  to  $40^{\circ}\text{C}$   
 4. CS2 controls address buffer, WE buffer,  $\overline{CS1}$  buffer,  $\overline{OE}$  buffer, and Din buffer. If CS2 controls data retention mode,  $V_{in}$  levels (address, WE,  $\overline{OE}$ ,  $\overline{CS1}$ , I/O) can be in the high impedance state. If  $\overline{CS1}$  controls data retention mode, CS2 must be  $CS2 \geq V_{CC} - 0.2\text{V}$  or  $0\text{V} \leq CS2 \leq 0.2\text{V}$ . The other input levels (address, WE,  $\overline{OE}$ , I/O) can be in the high impedance state.

Low  $V_{CC}$  Data Retention Timing Waveform (1) ( $\overline{CS1}$  Controlled)



Low  $V_{CC}$  Data Retention Timing Waveform (2) ( $CS2$  Controlled)

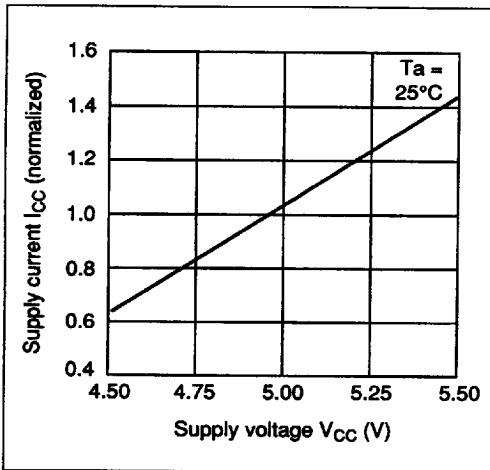


5

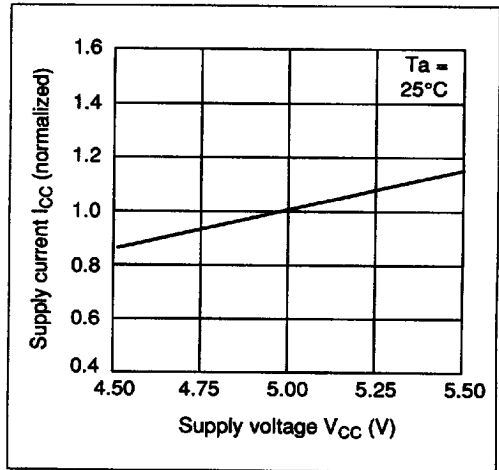
4496203 0024963 167 HITACHI

Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

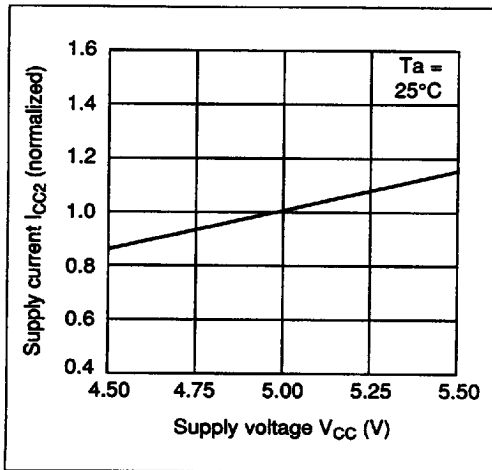
5-49



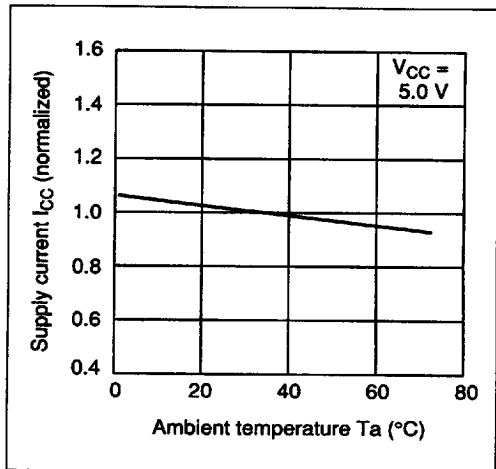
**Supply Current vs. Supply Voltage (1)**



**Supply Current vs. Supply Voltage (2)**



**Supply Current vs. Supply Voltage (3)**



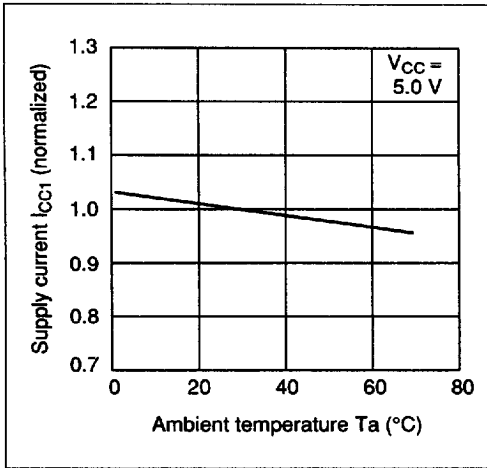
**Supply Current vs. Ambient Temperature (1)**

4496203 0024984 0T3

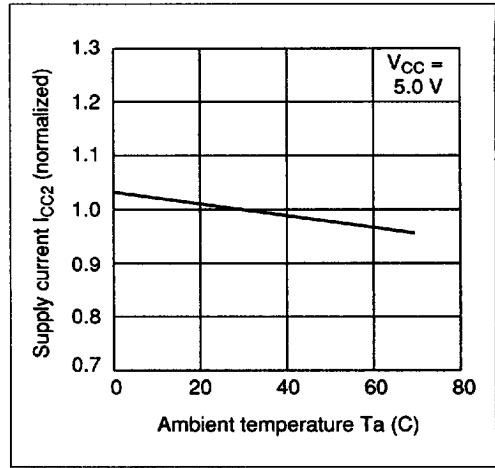
**HITACHI**

5-50

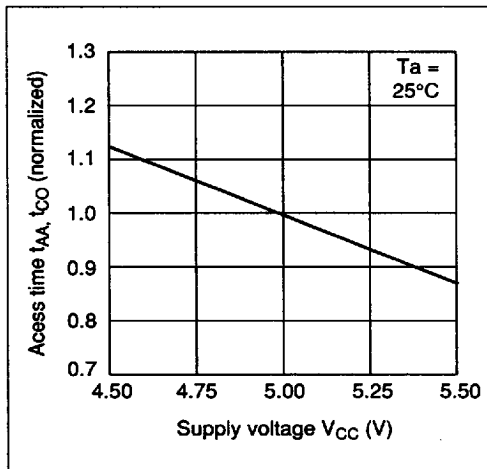
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300



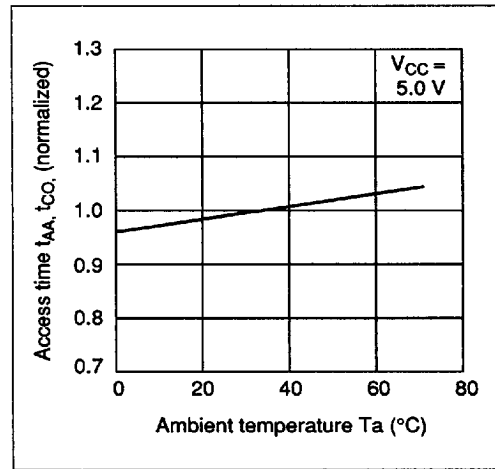
Supply Current vs. Ambient Temperature (2)



Supply Current vs. Ambient Temperature (3)

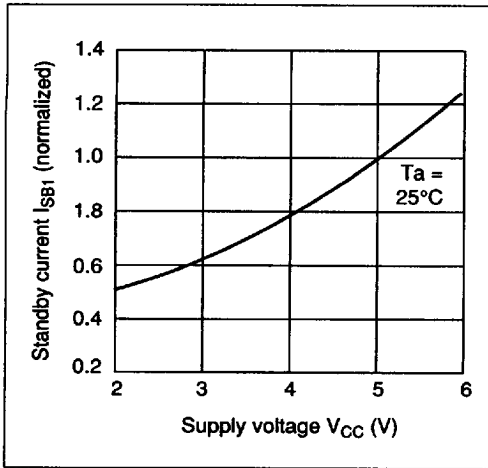


Access Time vs. Supply Voltage

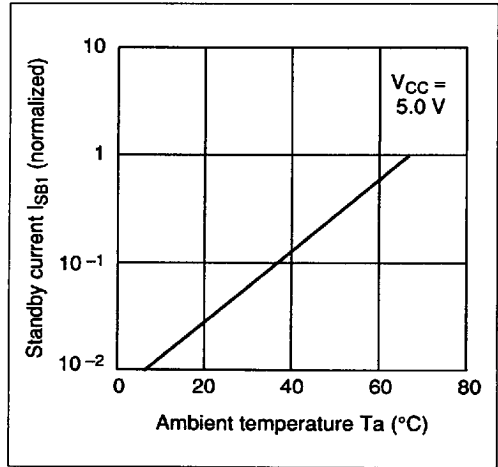


Access Time vs. Ambient Temperature

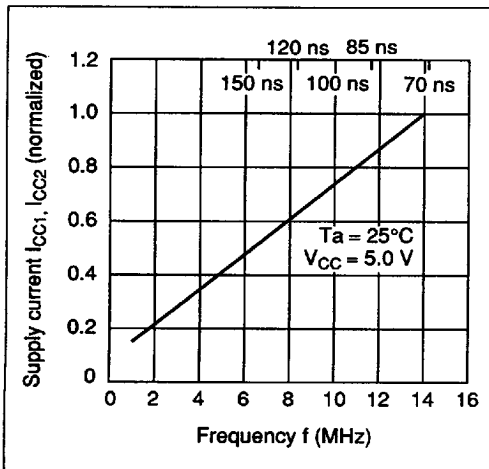
5



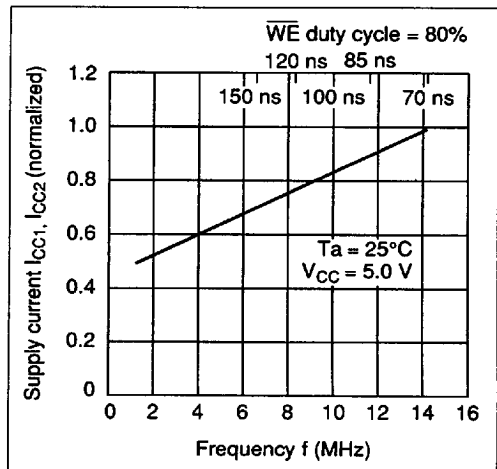
Standby Current vs. Supply Voltage



Standby Current vs. Ambient Temperature



Supply Current vs. Frequency (Read)



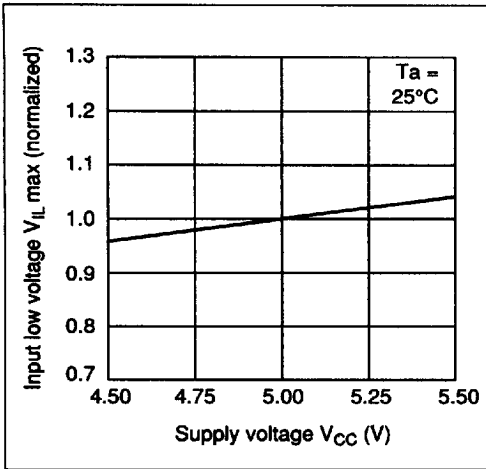
Supply Current vs. Frequency (Write)

4496203 0024986 976

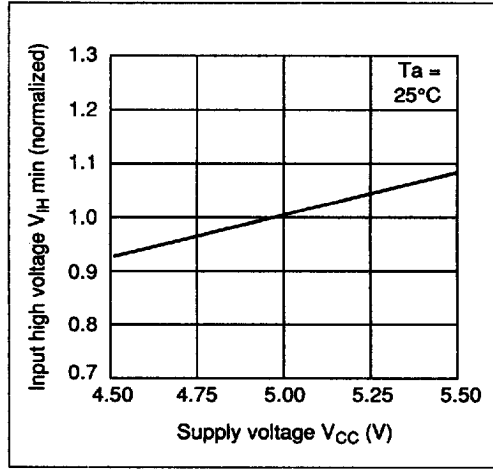
HITACHI

5-52

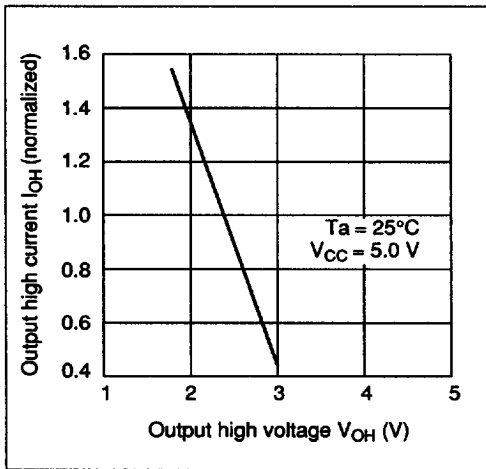
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300



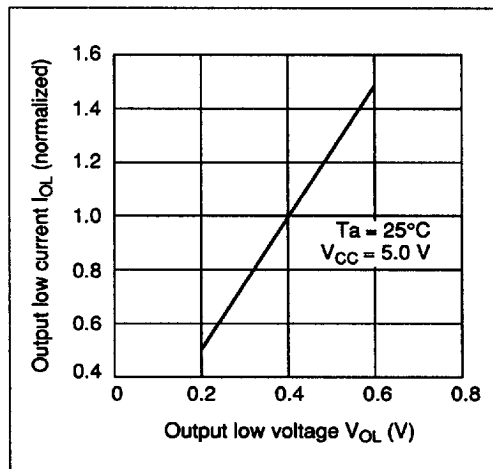
Input Low Voltage vs. Supply Voltage



Input High Voltage vs. Supply Voltage

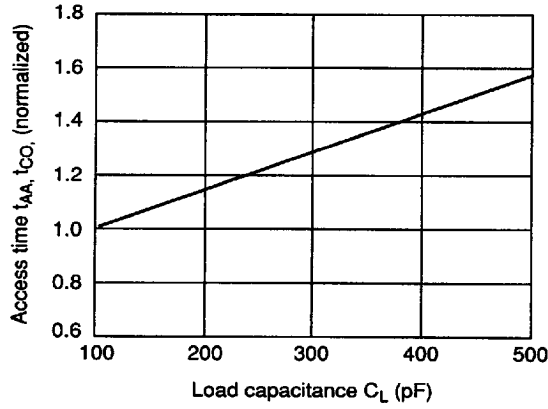


Output High Current vs. Output High Voltage



Output Low Current vs. Output Low Voltage

5



Access Time vs. Load Capacitance

4496203 0024988 749

HITACHI

5-54

Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300