PIC18F2585/2680/4585/4680 Rev. A1 Silicon/Data Sheet Errata

The PIC18F2585/2680/4585/4680 Rev. A1 parts you have received conform functionally to the Device Data Sheet (DS39625**B**), except for the anomalies described below.

Microchip intends to address all issues listed here in future revisions of the PIC18F2585/2680/4585/4680 silicon.

The following silicon errata apply only to PIC18F2585/2680/4585/4680 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2585	01 1010 100	00010
PIC18F2680	01 1010 110	00010
PIC18F4585	01 1010 101	00010
PIC18F4680	01 1010 111	00010

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: ECCP

When monitoring a shutdown condition using a bit test on the ECCPASE bit (ECCP1AS<7>), or performing a bit operation on the ECCPASE bit, the device may produce unexpected results.

Work around

Before performing a bit test or bit operation on the ECCPASE bit, copy the ECCP1AS register to the working register and perform the operation there.

By avoiding these operations on the ECCPASE bit in the ECCP1AS register, the module will operate normally.

In Example 1, ECCPASE bit operations are performed on the W register.

EXAMPLE 1:

```
MOVF    ECCP1AS, W
BTFSC   WREG, ECCPASE
BRA     SHUTDOWN_ROUTINE
```

2. Module: ECCP

When a shutdown condition occurs, the output port is made inactive for the duration of the event. After the event that caused the shutdown ends, the ECCP module enables the PWM output right away instead of waiting until the beginning of the next PWM cycle.

Work around

Disable the auto-restart feature in software, polling the Timer2 Interrupt Flag "TMR2IF" and wait until it is set before clearing the ECCPASE bit.

3. Module: ECCP

ECCP1 configured for auto-shutdown with Comparator 1 corrupts the PWM duty cycle pulse. In addition, it does not always synchronize the pulse to the beginning of the period and the end of the pulse can occur at any time within the period.

Work around

None.

4. Module: ECCP

The auto-shutdown event will cause the ECCP pins (P1A, P1B, P1C, P1D) to draw higher current than expected. This occurs when the ECCPAS1 or ECCPAS0 bits are set and an auto-shutdown event occurs.

Work around

None.

5. Module: ECCP

The auto-shutdown source, FLT0, has inverse polarity from the description in **Section 16.4.7 "Enhanced PWM Auto-Shutdown"** of the Device Data Sheet. A logic high-voltage level on FLT0 will generate a shutdown on ECCP1.

Work around

Invert the logic in the program's source code.

6. Module: ECCP

If a Halt command is issued while debugging with the In-Circuit Debugger (MPLAB® ICD 2), the ECCP module may freeze completely. However, if a shutdown is enabled and triggered by the FLT0 pin, the ECCPASE bit is set and the outputs are driven to their shutdown state, as defined by the PSSAC1:PSSAC0 and PSSBD1:PSSBD0 bits, regardless of the debugging process being stopped.

Work around

None.

7. Module: ECCP

In 10-bit Addressing mode, when a Repeated Start is issued followed by the high address byte and a write command, an ACK is not issued.

Work around

There are two workarounds available:

1. Single-Master Environment:
   In a single-master environment, the user must issue a Stop, then a Start, followed by a write to the address high, then the address low followed by the data.
2. Multi-Master Environment:
   In a multi-master environment, the user must issue a Repeated Start, send a dummy write command to a different address, issue another Repeated Start and then send a write to the original address. This procedure will prevent loss of the bus.

8. Module: ECCP and CCP

When ECCP1 and CCP2 are configured for PWM mode with 1:1 Timer2 prescaler and duty cycle set to the period minus 1, this may result in the PWM output(s) remaining at a logic low level.

Clearing the PR2 register to select the fastest period may also result in the output(s) remaining at a logic low output level.

Work around

To ensure a reliable waveform, verify that the selected duty cycle does not equal the 10-bit period minus 1 prior to writing these locations, or use 1:4 or 1:16 Timer2 prescale. Also, verify the PR2 register is not written to 00h.

All other duty cycle and period settings will function as described in the Device Data Sheet.

The ECCP and CCP modules remain capable of 10-bit accuracy.

9. Module: Timer1/Timer3

When Timer1 or Timer3 is configured for external clock source and the CCP1CON or ECCP1CON register is configured with 0x0B (Compare mode, trigger special event), the timer is not reset on a Special Event Trigger.

Work around

Modify firmware to reset the Timer registers upon detection of the compare match condition – TMRxL and TMRxH.

10. Module: Timer1/Timer3

When the Timer1/Timer3 is in External Clock Synchronized mode and the external clock period is between 1 and 2 TCY, interrupts may occasionally be skipped.

Work around

None.

11. Module: MSSP

When the MSSP is configured for SPI™ Master mode, the SDO pin cannot be disabled by setting the TRISC<5> bit. The SDO pin always outputs the content of SSPBUF regardless of the state of the TRIS bit.

In Slave mode with Slave Select enabled, SSPM3:SSPM0 = `0010` (SSPCON<3:0>), the SDO pin can be disabled by placing a logic high level on the $\overline{SS}$ pin (RA5).

Work around

None.

12. Module: MSSP

After an I^2C™ transfer is initiated, the SSPBUF register may be written for up to 10 TCY before additional writes are blocked. The data transfer may be corrupted if SSPBUF is written during this time.

The WCOL bit is set any time an SSPBUF write occurs during a transfer.

Work around

Avoid writing SSPBUF until the data transfer is complete, indicated by the setting of the SSPIF bit (PIR1<3>).

Verify the WCOL bit (SSPCON1<7>) is clear after writing SSPBUF to ensure any potential transfer in progress is not corrupted.

13. Module: MSSP

In its current implementation, the I^2C™ Master mode operates as follows:

a) The Baud Rate Generator for I^2C in Master mode is slower than the rates specified in Table 17-3 of the Device Data Sheet.

For this revision of silicon, use the values shown in Table 1 in place of those shown in Table 17-3 of the Device Data Sheet. The differences are shown in **bold** text.

b) Use the following formula in place of the one shown in Register 17-4 (SSPCON1) of the Device Data Sheet for bit description, SSPM3:SSPM0 = `1000`.

SSPADD = INT((FCY/FSCL) – (FCY/1.111 MHz)) – 1

TABLE 1: I^2C™ CLOCK RATE w/BRG

FOSC	FCY	FCY*2	BRG Value	FSCL (2 Rollovers of BRG)
40 MHz	10 MHz	20 MHz	**0Eh**	400 kHz(1)
40 MHz	10 MHz	20 MHz	**15h**	312.5 kHz
40 MHz	10 MHz	20 MHz	**59h**	100 kHz
16 MHz	4 MHz	8 MHz	**05h**	400 kHz(1)
16 MHz	4 MHz	8 MHz	**08h**	308 kHz
16 MHz	4 MHz	8 MHz	**23h**	100 kHz
4 MHz	1 MHz	2 MHz	**01h**	333 kHz(1)
4 MHz	1 MHz	2 MHz	**08h**	100 kHz
4 MHz	1 MHz	2 MHz	00h	1 MHz(1)

Note 1: The I^2C™ interface does not conform to the 400 kHz I^2C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

14. Module: MSSP

RCEN becomes set when the system is Idle. In normal operation, the setting of RCEN should be ignored by the module while the system is not Idle.

Work around

Wait for the system to become Idle. This requires a check for the following bits to be reset:

ACKEN, RCEN, PEN, RSEN and SEN.

15. Module: A/D

The A/D offset is greater than the specified limit in Table 27-24 of the Device Data Sheet. The addition of Parameter A06A and updated conditions and limits are shown in **bold** text in Table 2.

Work around

Three workarounds exist.

1. Configure the A/D to use the VREF+ and VREF- pins for the voltage references. This is done by setting the VCFG<1:0> bits (ADCON1<5:4>).
2. Perform a conversion on a known voltage reference voltage and adjust the A/D result in software.
3. Increase system clock speed to 40 MHz and adjust A/D settings accordingly. Higher system clock frequencies decrease offset error.

TABLE 2: A/D CONVERTER CHARACTERISTICS: PIC18F2585/2680/4585/4680 (INDUSTRIAL) PIC18LF2585/2680/4585/4680 (INDUSTRIAL)

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
A06A	**EOFF**	**Offset Error**	**—**	**—**	**<±1.5**	**LSb**	**VREF = VREF+ and VREF-**
A06	EOFF	Offset Error	—	—	**<±-3.5**	LSb	**VREF = VSS and VDD**

16. Module: DC Characteristics (BOR)

The values for parameter D005 (VBOR) in **Section 27.1 "DC Characteristics: Supply Voltage"** of the Device Data Sheet, when the trip point for BORV1:BORV0 = 11, are not applicable as the device may reset below the minimum operating voltage for the device.

Work around

None.

17. Module: BOD/HLVD

Due to production tolerances, selecting the lowest setting for Brown-out Detect (BORV1:BORV0 = 11) or Low-Voltage Reset (LVV = 0000) is not recommended, since it may result in an actual Brown-out Reset or Low-Voltage Detect below the minimum allowable VDD of 2.0V.

Work around

Use the next highest BOD or HLVD voltage threshold to ensure a low VDD is detected before it drops below 2.0V.

18. Module: ECCP

When operating either Timer1 or Timer3 as a counter with a prescale value other than 1:1 and operating the ECCP in Compare mode with the Special Event Trigger (CCP1CON bits CCP1M3:CCP1M0 = 1011), the Special Event Trigger Reset of the timer occurs as soon as there is a match between TMRxH:TMRxL and CCPR1H:CCPR1L.

This differs from the PIC18F458, where the Special Event Trigger Reset of the timer occurs on the next rollover of the prescale counter, after the match between TMRxH:TMRxL and CCPR1H:CCPR1L.

Work around

To achieve the same timer Reset period on the PIC18F4680 family as the PIC18F458 family for a given clock source, add 1 to the value in CCPR1H:CCPR1L. In other words, if CCPR1H:CCPR1L = x for the PIC18F458, to achieve the same Reset period on the PIC18F4680 family, CCPR1H:CCPR1L = x + 1, where the prescale is 1, 2, 4 or 8 depending on the T1CKPS1:T1CKPS0 bit values.

19. Module: Interrupts

If a high priority interrupt occurs during a two-cycle instruction that modifies the STATUS, BSR or WREG register, the unmodified value of the register will be saved to the corresponding Fast Return (Shadow) register and upon a fast return from the interrupt, the unmodified value will be restored to the STATUS, BSR or WREG register.

For example, if a high priority interrupt occurs during the instruction, `MOVFF TEMP, WREG`, the `MOVFF` instruction will be completed and WREG will be loaded with the value of `TEMP` before branching to ISR. However, the previous value of WREG will be saved to the Fast Return register during ISR branching. Upon return from the interrupt with a fast return, the previous value of WREG in the Fast Return register will be written to WREG. This results in WREG containing the value it had before execution of `MOVFF TEMP, WREG`.

Affected instructions are:

`MOVFF Fs, Fd`
where `Fd` is WREG, BSR or STATUS;

`MOVSF Zs, Fd`
where `Fd` is WREG, BSR or STATUS; and

`MOVSS [Zs], [Zd]`
where the destination is WREG, BSR or STATUS.

Work around

1. Assembly Language Programming: If any two-cycle instruction is used to modify the WREG, BSR or STATUS register, do not use the `RETFIE FAST` instruction to return from the interrupt. Instead, save/restore WREG, BSR and STATUS via software in the same manner as is done with low priority interrupts. Alternatively, in the case of `MOVFF`, use the `MOVF` instruction to write to WREG instead.
2. C Language Programming: The exact work around depends on the compiler in use. Please refer to your C Compiler documentation for details.

   If using the Microchip MPLAB® C18 C Compiler, define both high and low priority interrupt handler functions as “low priority” by using the `pragma interruptlow` directive. This directive instructs the compiler to not use the `RETFIE FAST` instruction. If the proper high priority interrupt bit is set in the IPRx register, then the interrupt is treated as high priority in spite of the `pragma interruptlow` directive.

   The following code snippet demonstrates the work around using the C18 compiler:

```
#pragma interruptlow MyLowISR
void MyLowISR(void)
{
    // Handle low priority interrupts.
}

// Although MyHighISR is a high priority interrupt, use interruptlow pragma so that
// the compiler will not use retfie FAST.

#pragma interruptlow MyHighISR
void MyHighISR(void)
{
    // Handle high priority interrupts.
}

#pragma code highVector=0x08
void HighVector (void)
{
    _asm goto MyHighISR _endasm
}
#pragma code /* return to default code section */

#pragma code lowhVector=0x18
void LowVector (void)
{
    _asm goto MyLowISR _endasm
}
#pragma code /* return to default code section */
```

20. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTA register is set), an ongoing transmission's timing can be corrupted if the TX9D bit (for the next transmission) is not written immediately following the setting of TXIF. This is because any write to the TXSTA register results in a reset of the Baud Rate Generator which will effect any ongoing transmission.

Work around

Load TX9D just after TXIF is set, either by polling TXIF or by writing TX9D at the beginning of the Interrupt Service Routine, or only write to TX9D when a transmission is not in progress (TRMT = 1).

21. Module: Timer1/Timer3

When Timer1/Timer3 is operating in 16-bit mode and the prescale setting is not 1:1, a write to the TMR1H/TMR3H Buffer registers may lengthen the duration of the period between the increments of the timer for the period in which TMR1H/TMR3H was written. It does not change the actual prescale value.

Work around

Do not write to TMR1H/TMR3H while Timer1/Timer3 is running, or else write to TMR1L/TMR3L immediately following a write to TMR1H/TMR3H.

Do not write to TMR1H/TMR3H and then wait for another event before also updating TMR1L/TMR3L.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39625**B**), the following clarifications and corrections should be noted.

1. Module: DC Characteristics

The following parameters in **Section 27.3 "DC Characteristics"** have been updated as follows:

- D031, D041 – references to RC3 and RC4 were removed
- D032A has been renamed D033
- D033 has been renamed D033A
- D042A has been renamed D043
- D043 has been renamed D043A
- D034, D043B, D043C and D044 have been added

Changes are shown in **bold** text in the following table.

27.3 DC Characteristics: PIC18F2585/2680/4585/4680 (Industrial) PIC18LF2585/2680/4585/4680 (Industrial)

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**				
		I/O ports:				
D030		with TTL buffer	VSS	0.15 VDD	V	VDD < 4.5V
D030A			—	0.8	V	4.5V ≤ VDD ≤ 5.5V
D031		with Schmitt Trigger buffer	VSS	0.2 VDD	V	
D032		$\overline{MCLR}$	VSS	0.2 VDD	V	
D033		**OSC1**	**VSS**	**0.3 VDD**	**V**	**HS, HSPLL modes**
D033A		**OSC1**	**VSS**	**0.2 VDD**	**V**	**RC, EC modes(1)**
D033B		**OSC1**	**VSS**	**0.3 VDD**	**V**	**XT, LP modes**
D034		**T13CKI**	**VSS**	**0.3 VDD**	**V**	
	VIH	**Input High Voltage**				
		I/O ports:				
D040		with TTL buffer	0.25 VDD + 0.8V	VDD	V	VDD < 4.5V
D040A			2.0	VDD	V	4.5V ≤ VDD ≤ 5.5V
D041		with Schmitt Trigger buffer	0.8 VDD	VDD	V	
D042		$\overline{MCLR}$	0.8 VDD	VDD	V	
D043		**OSC1**	**0.7 VDD**	**VDD**	**V**	**HS, HSPLL modes**
D043A		**OSC1**	**0.8 VDD**	**VDD**	**V**	**EC mode**
D043B		**OSC1**	**0.9 VDD**	**VDD**	**V**	**RC mode(1)**
D043C		**OSC1**	**1.6**	**VDD**	**V**	**XT, LP modes**
D044		**T13CKI**	**1.6**	**VDD**	**V**	

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PICmicro® device be driven with an external clock while in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: Parameter is characterized but not tested.

2. Module: MOVFF Instruction

In the MOVFF instruction description, there is an error. The description should read: “Cycles: 2” rather than “Cycles: 2 (3)”. Changes are shown in **bold** text in the following table.

MOVFF	**Move f to f**			
Syntax:	MOVFF f_s,f_d			
Operands:	$0 \le f_s \le 4095$ $0 \le f_d \le 4095$			
Operation:	$(f_s) \rightarrow f_d$			
Status Affected:	None			
Encoding:				
1st word (source)	1100	ffff	ffff	fffff_s
2nd word (destin.)	1111	ffff	ffff	fffff_d
Description:	The contents of source register ‘f_s’ are moved to destination register ‘f_d’. Location of source ‘f_s’ can be anywhere in the 4096-byte data space (000h to FFFh) and location of destination ‘f_d’ can also be anywhere from 000h to FFFh. Either source or destination can be W (a useful special situation). MOVFF is particularly useful for transferring a data memory location to a peripheral register (such as the transmit buffer or an I/O port). The MOVFF instruction cannot use the PCL, TOSU, TOSH or TOSL as the destination register			
Words:	2			
Cycles:	**2**			

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register ‘f’ (src)	Process Data	No operation
Decode	No operation No dummy read	No operation	Write register ‘f’ (dest)

Example: MOVFF REG1, REG2

Before Instruction
REG1 = 33h
REG2 = 11h
After Instruction
REG1 = 33h
REG2 = 33h

REVISION HISTORY

Rev A Document (9/2004)

First revision of this document which includes silicon issues 1-7 (ECCP), 8 (ECCP and CCP), 9-10 (Timer1/ Timer3), 11-14 (MSSP), 15 (A/D), 16 (DC Characteristics – BOR) and 17 (BOD/HLVD). Added data sheet clarification issue 1 (DC Characteristics) and 2 (MOVFF Instruction).

Rev B Document (11/2004)

Added silicon issues 18 (ECCP), 19 (Interrupts), 20 (EUSART) and 21 (Timer1/Timer3).

NOTES:

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